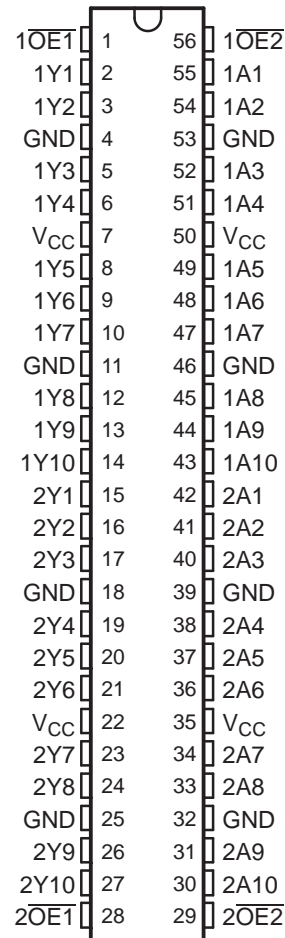


## FEATURES

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree <sup>(1)</sup>
- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DGG OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION

This 20-bit noninverting buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ( $1\overline{OE}1$  and  $1\overline{OE}2$  or  $2\overline{OE}1$  and  $2\overline{OE}2$ ) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SSOP – DL	Tape and reel	CALVCH16827MDLREP	ALVCH16827EP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus, EPIC are trademarks of Texas Instruments.

**DESCRIPTION (CONTINUED)**

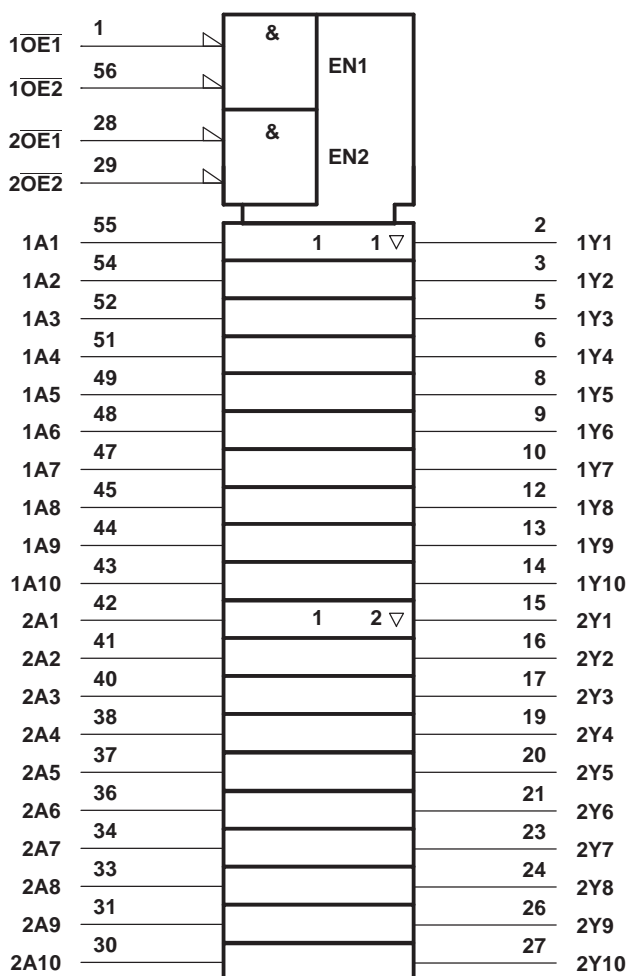
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16827-EP is characterized for operation from –55°C to 125°C.

**FUNCTION TABLE**  
**(each 10-bit section)**

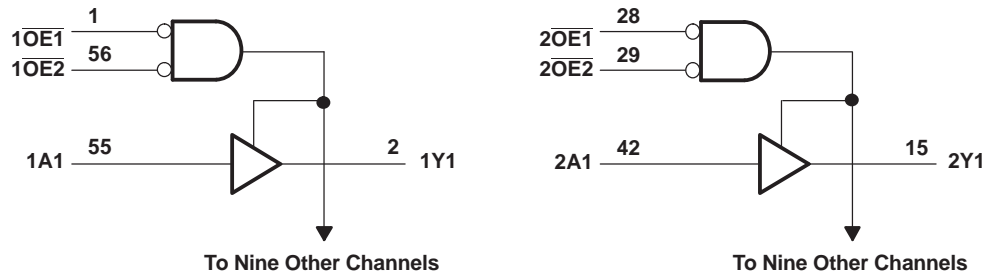
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

**LOGIC SYMBOL<sup>(1)</sup>**



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current			±50 mA
	Continuous current through each V <sub>CC</sub> or GND			±100 mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DL package		74 °C/W
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-4	mA
		V <sub>CC</sub> = 2.3 V	-12	
		V <sub>CC</sub> = 2.7 V	-12	
		V <sub>CC</sub> = 3 V	-24	

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74ALVCH16827-EP 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES676–SEPTEMBER 2006

## RECOMMENDED OPERATING CONDITIONS (continued)

		MIN	MAX	UNIT
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	12	
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature <sup>(2)</sup>	-55	125	°C

(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$	1.65 V to 3.6 V	$V_{CC} - 0.2$			V
	$I_{OH} = -4\ \text{mA}$	1.65 V	1.2			
	$I_{OH} = -6\ \text{mA}$	2.3 V	2			
	$I_{OH} = -12\ \text{mA}$	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24\ \text{mA}$	3 V	2			
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 3.6 V			0.2	V
	$I_{OL} = 4\ \text{mA}$	1.65 V			0.45	
	$I_{OL} = 6\ \text{mA}$	2.3 V			0.4	
	$I_{OL} = 12\ \text{mA}$	2.3 V			0.7	
		2.7 V			0.4	
$I_{OL} = 24\ \text{mA}$	3 V			0.55		
$I_I$	$V_I = V_{CC}$ or GND	3.6 V			±5	μA
$I_{I(\text{hold})}$	$V_I = 0.58\text{ V}$	1.65 V	25			μA
	$V_I = 1.07\text{ V}$	1.65 V	-25			
	$V_I = 0.7\text{ V}$	2.3 V	45			
	$V_I = 1.7\text{ V}$	2.3 V	-45			
	$V_I = 0.8\text{ V}$	3 V	75			
	$V_I = 2\text{ V}$	3 V	-75			
	$V_I = 0$ to 3.6 V <sup>(2)</sup>	3.6 V			±500	
$I_{OZ}$	$V_O = V_{CC}$ or GND	3.6 V			±10	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μA
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , $V_I$ Other inputs at $V_{CC}$ or GND	3 V to 3.6 V			750	μA
$C_i$	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		3.5	pF
	Data inputs				6	
$C_o$	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5	pF

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	(1)	1	5.1	4.9		1	4.4	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	(1)	1	7	6.7		1	5.7	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	(1)	1.2	6.6	5.9		1.3	5.5	ns

(1) This information was not available at the time of publication.

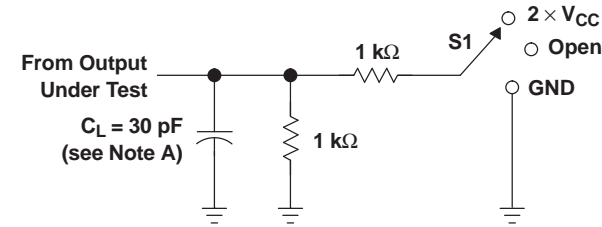
## OPERATING CHARACTERISTICS

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation	Outputs enabled	(1)	16	18	pF
	capacitance	Outputs disabled	(1)	4	6	

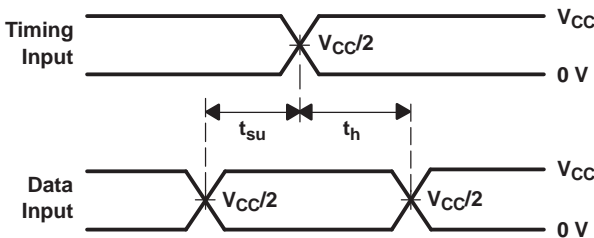
(1) This information was not available at the time of publication.

**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 1.8\text{ V}$

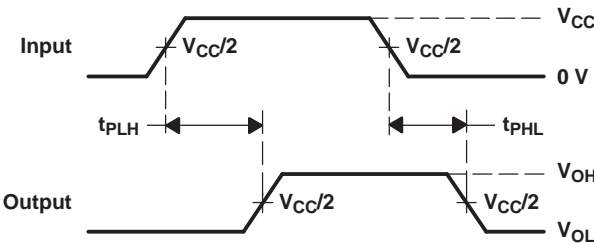


**LOAD CIRCUIT**

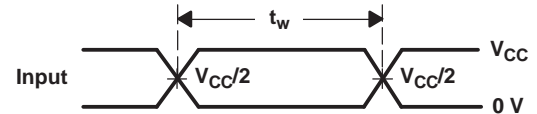
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



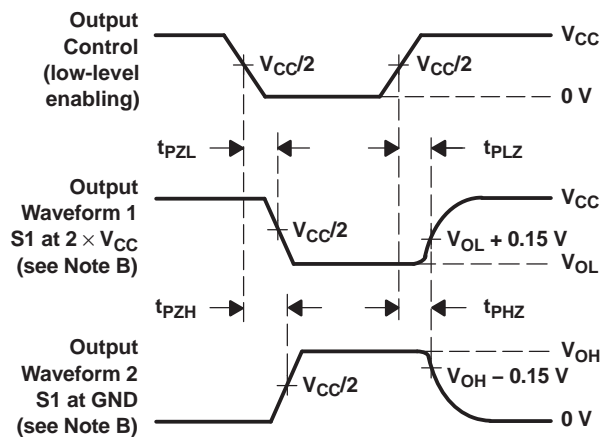
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



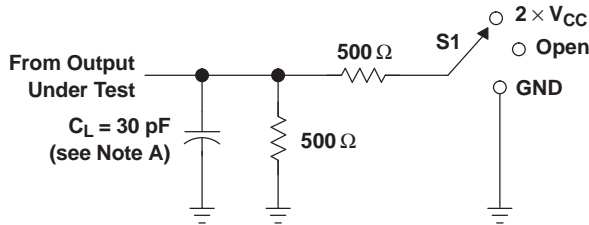
**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

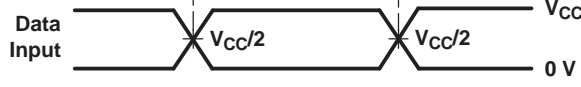
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$

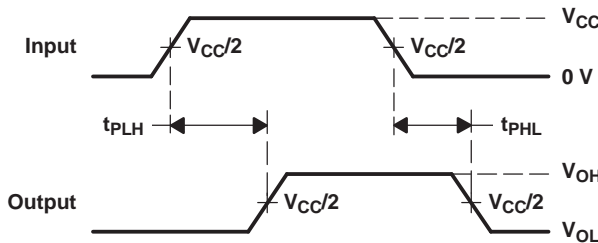


LOAD CIRCUIT

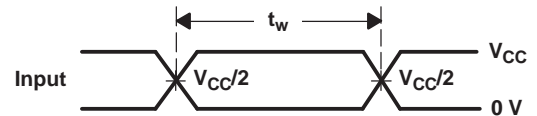
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



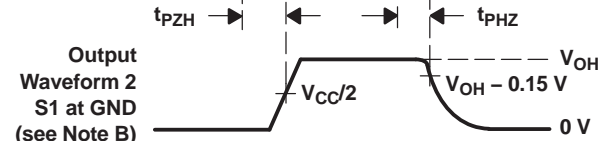
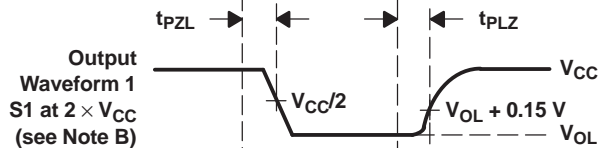
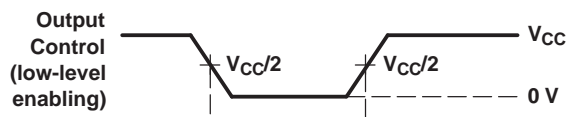
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION

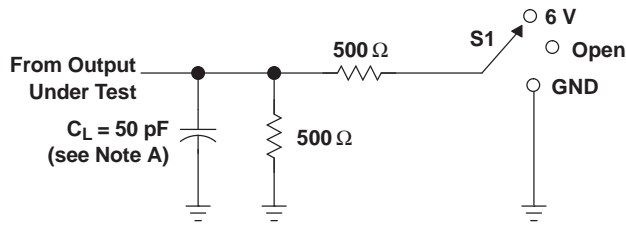


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

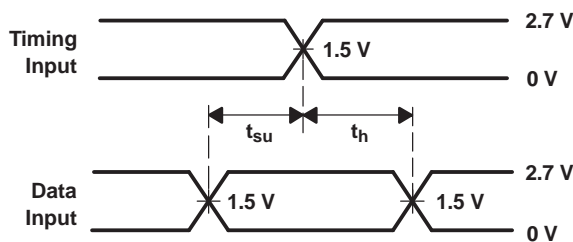
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

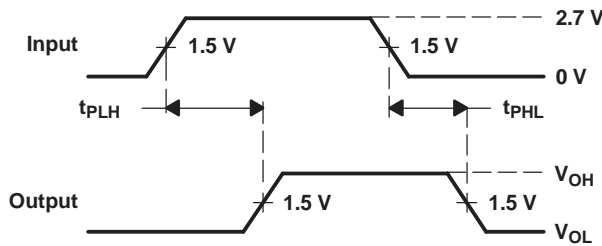


LOAD CIRCUIT

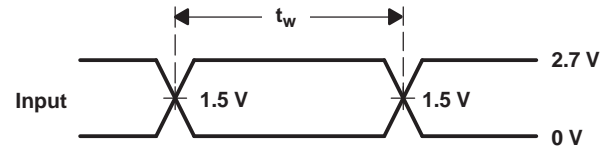
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



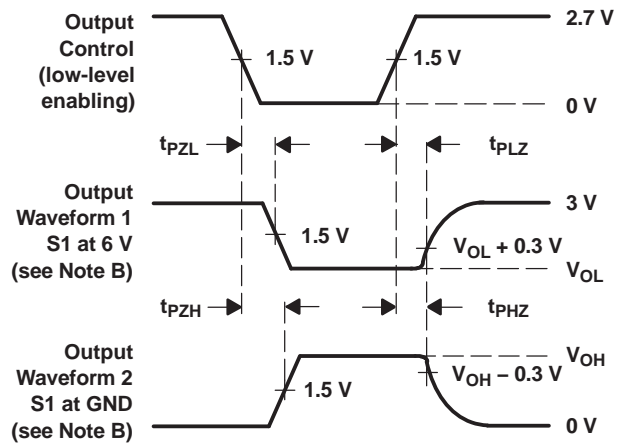
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CALVCH16827MDLREP	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06679-01XE	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN74ALVCH16827-EP :**

- Catalog: [SN74ALVCH16827](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CALVCH16827MDLREP	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CALVCH16827MDLREP	SSOP	DL	56	1000	346.0	346.0	49.0

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